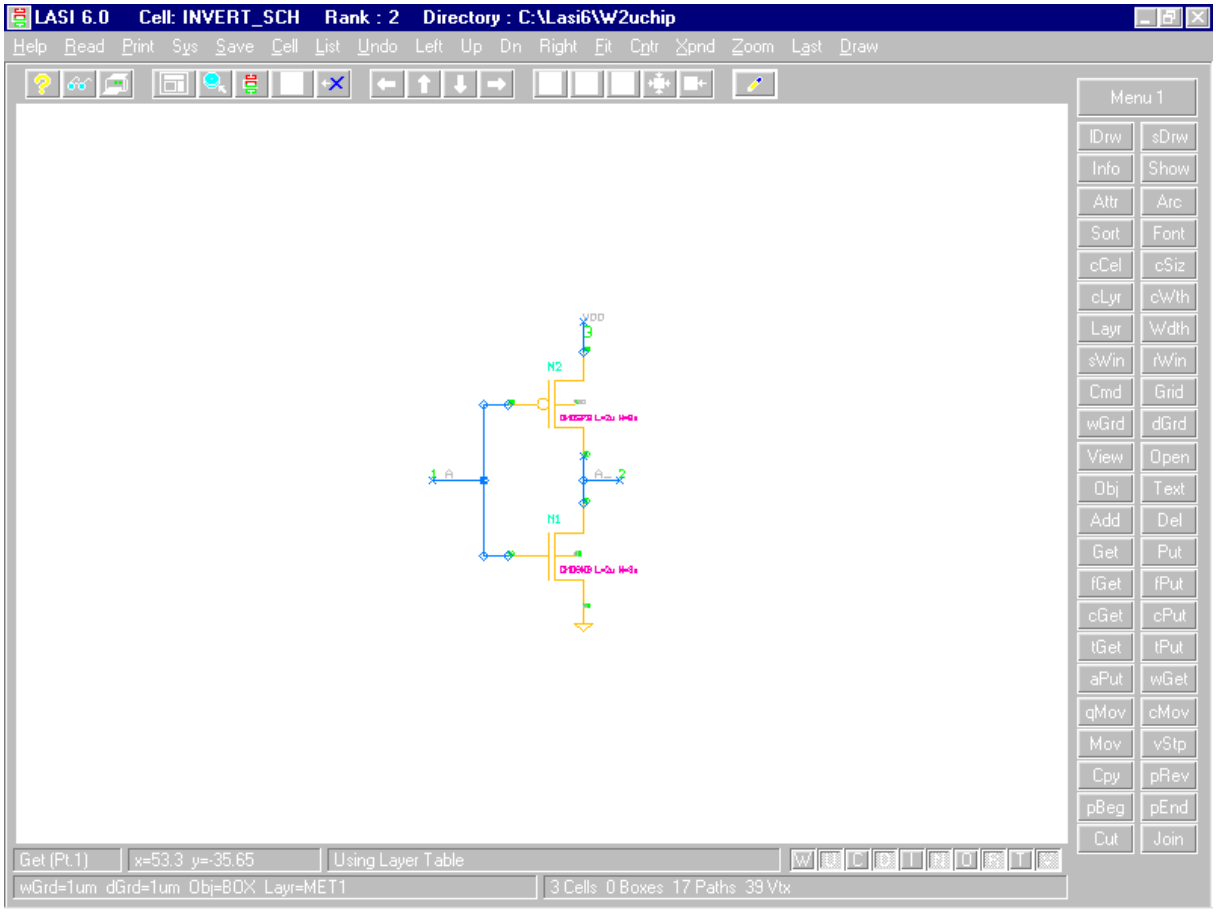
There are many ways of making schematic symbols using LASI. We will show a simple method here using the setups provided in the C:\LASI6\W2uchip directory (the example chip design that uses the MOSIS design rules and Orbit's (now Supertex) 2 um process.

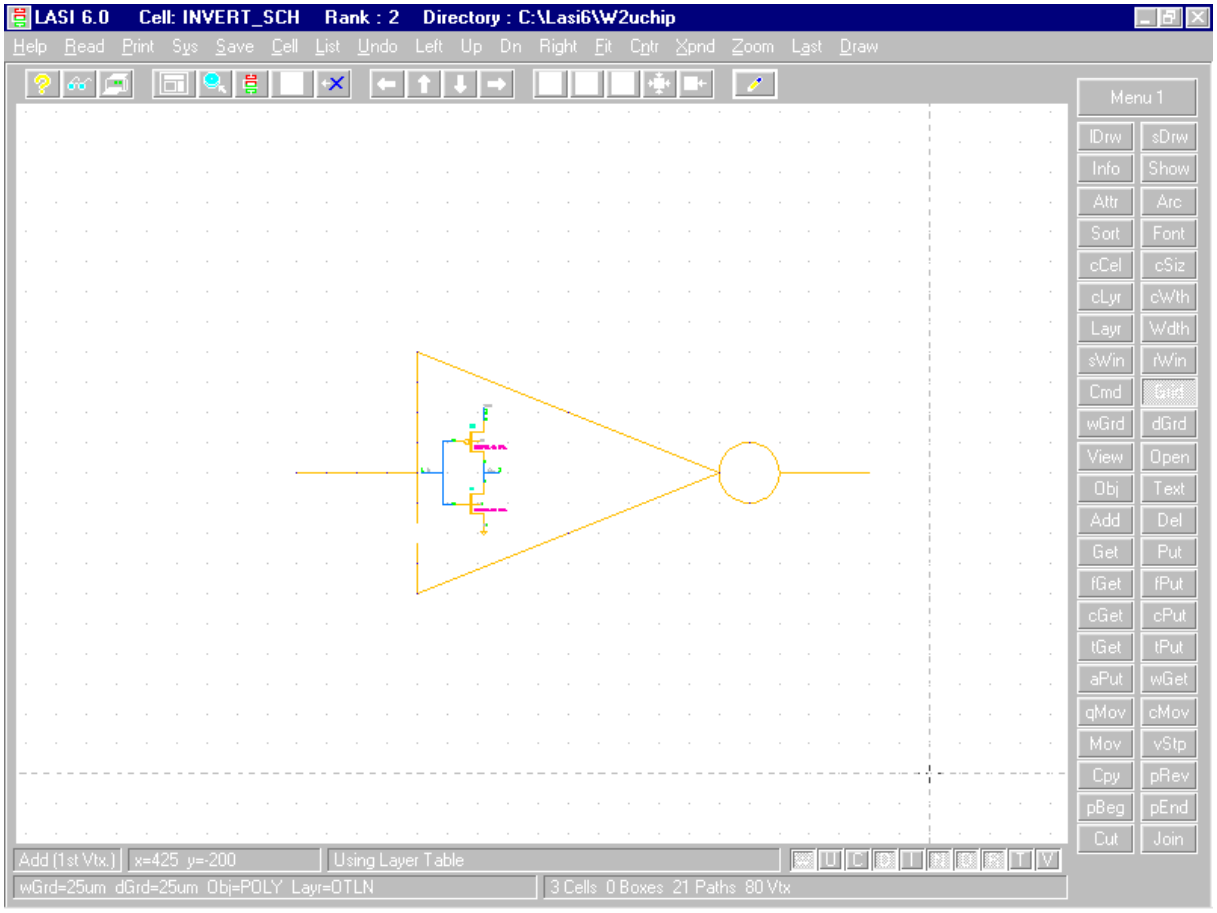
Consider the basic inverter transistor schematic shown below. Let's make a symbol for this schematic. We begin by noticing the height of the cell is around 50 um. Note that dimensions in schematics are meaningless, unlike layout. What we're going to do is make our symbols on a larger grid and then use the **View** command to only show the layers we are interested in when displaying our symbol level schematics.

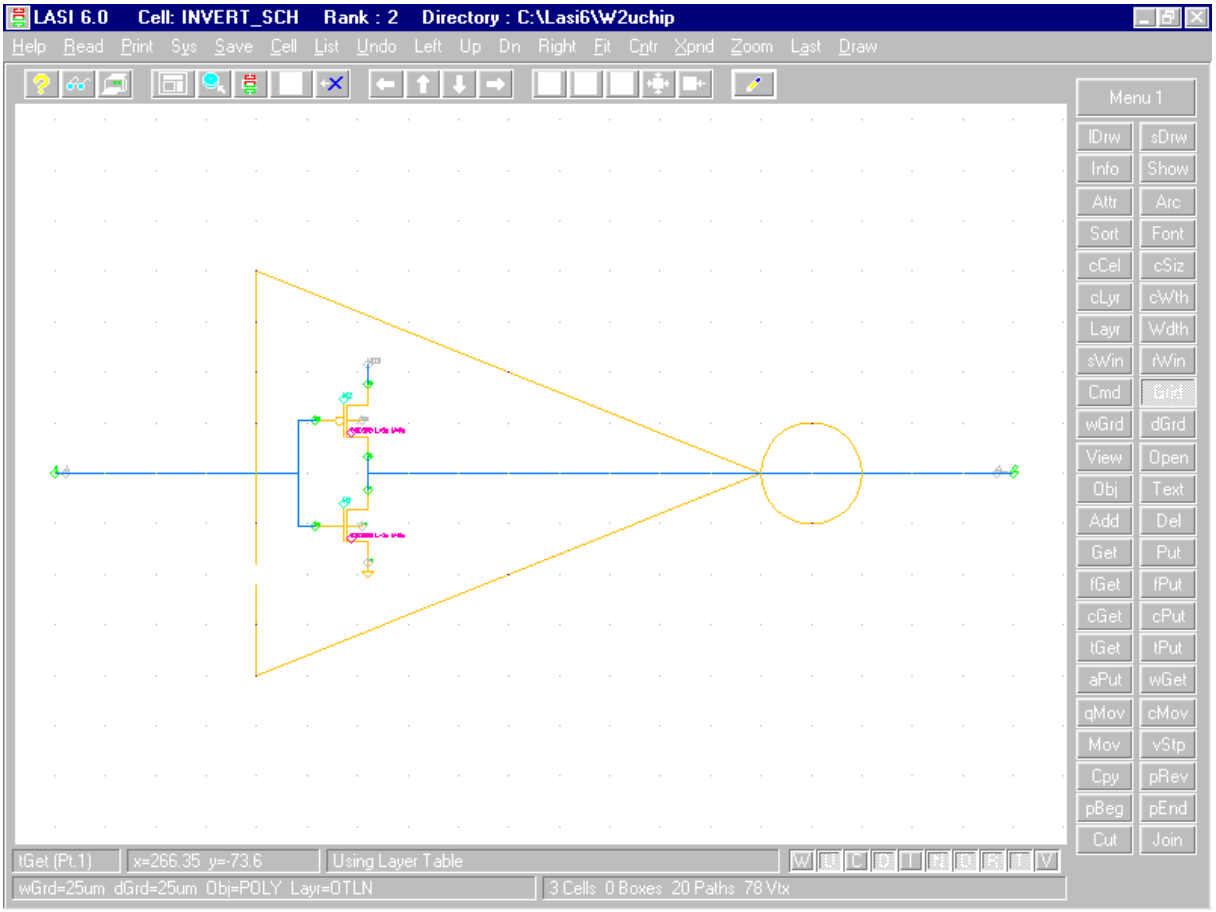


Next, using the **Set** command, set a working and unit grid to 50 um and then make these grids the active grid in LASI. We will make our small symbols, such as the inverter 200 um in height, while medium symbols, for example a D- Flip Flop will be 600 um, etc.

Next, set the object to a polygon and the layer to OTLN (outline). Draw, using the **Add** command, the symbol that you want for the circuit. For the example here, the result is shown on the top of the next page. Note that a 25 um grid was also used to make the circle (see problem 1.10 on page 21) and the inverter schematic was repositioned in the cell.

The next thing we need to do is move the connector text and wires (drawn on the metal1 layer) to the input and output of the cell. The result is seen in the next figure.


LASI 6.0 Cell: INVERT_SCH Rank : 2 Directory : C:\Lasi6\W2uchip
Help Read Print Sys Save Cell List Undo Left Up Dn Right Fit Cntr Xpnd Zoom Last Draw
Menu 1
lDrw sDrw
Info Show
Attr Arc
Sort Font
cCel cSiz
cLyr cWth
Layr Wdth
sWin rWin
Cmd Grid
wGrd dGrd
View Open
Obj Text
Add Del
Get Put
fGet fPut
cGet cPut
tGet tPut
aPut wGet
qMov cMov
Mov vStp
Cpy pRev
pBeg pEnd
Cut Join
Add (1st Vtx.)
x=425 y=-200
Using Layer Table
wGrd=25um dGrd=25um Obj=POLY Layr=OTLN
3 Cells 0 Boxes 21 Paths 80 Vtx


LASI 6.0 Cell: INVERT_SCH Rank : 2 Directory : C:\Lasi6\W2uchip
Help Read Print Sys Save Cell List Undo Left Up Dn Right Fit Cntr Xpnd Zoom Last Draw
Menu 1
lDrw sDrw
Info Show
Attr Arc
Sort Font
cCel cSiz
cLyr cWth
Layr Wdth
sWin rWin
Cmd Grid
wGrd dGrd
View Open
Obj Text
Add Del
Get Put
fGet fPut
cGet cPut
tGet tPut
aPut wGet
qMov cMov
Mov vStp
Cpy pRev
pBeg pEnd
Cut Join
tGet (Pt.1)
x=266.35 y=-73.6
Using Layer Table
wGrd=25um dGrd=25um Obj=POLY Layr=OTLN
3 Cells 0 Boxes 20 Paths 78 Vtx

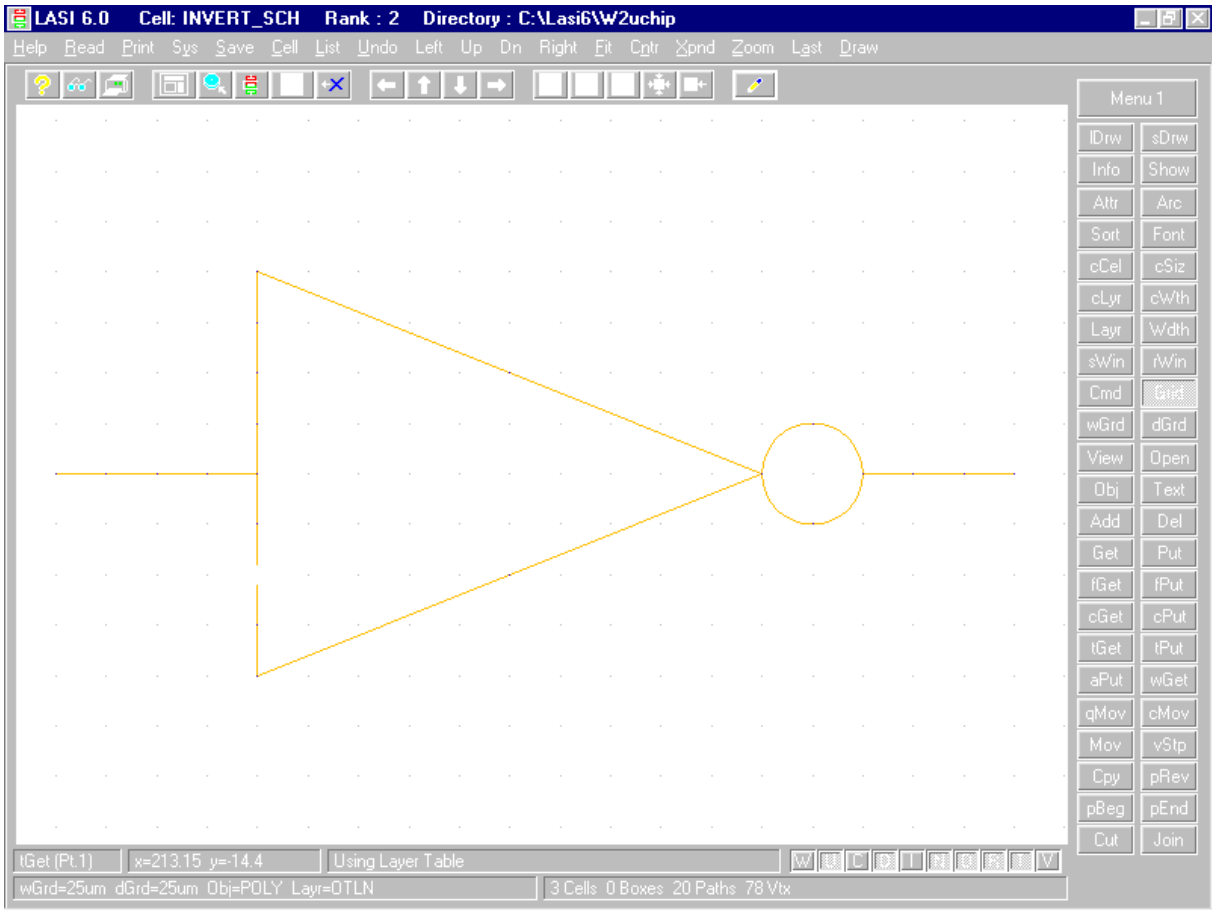
Note that switching from one grid to another may be useful (or simply not snapping to the grids by pressing the “a” on the keyboard) when doing the drawings.

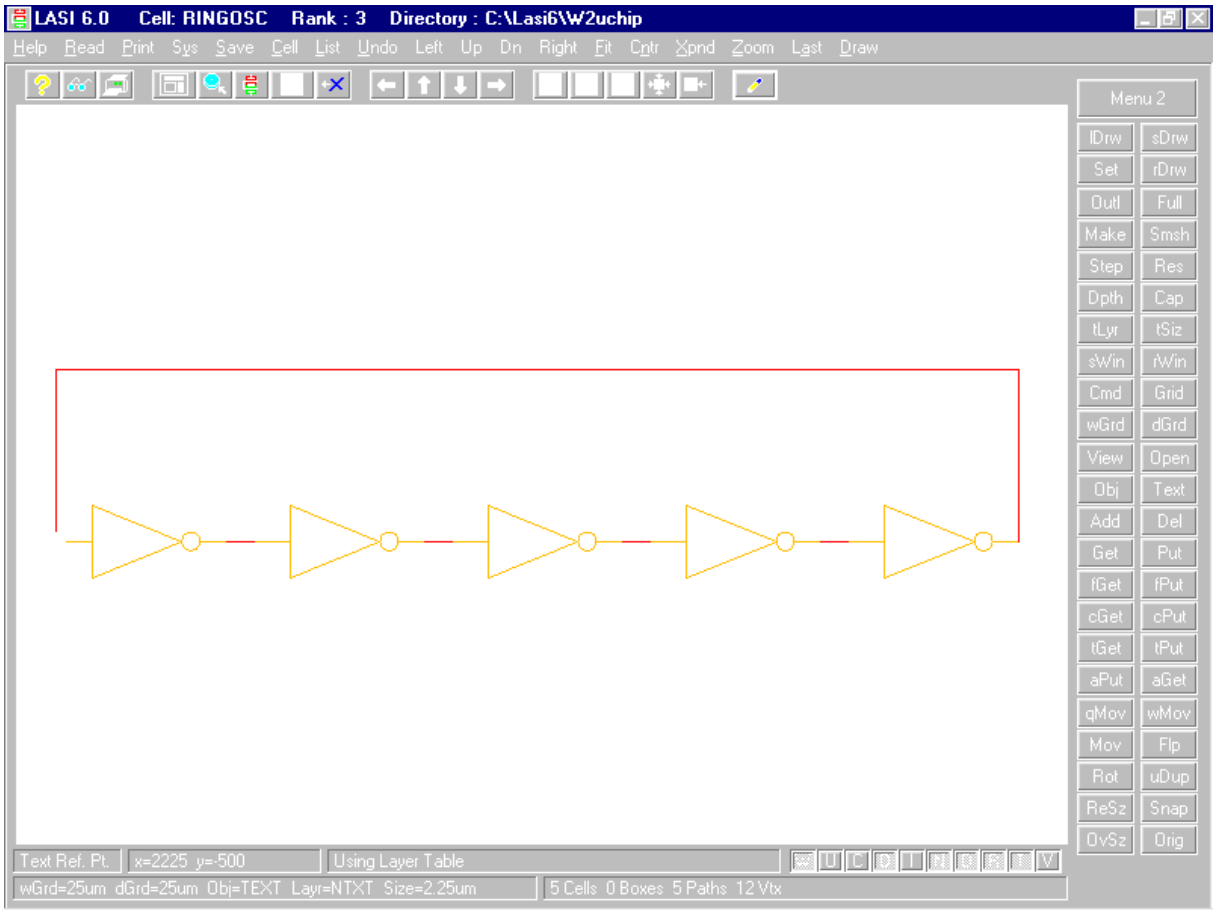
Also note that the VDD connector text on the symbol has been deleted. It can be added but since VDD is, generally, a global symbol it’s much easier to just add

.global VDD

to the spice netlist. Note that the node text indicating VDD has not been removed.

Use the **View** layers to show only the layers of interest, for example, OTLN and the wire used on the symbol layer schematics. Since Metal1 is used on the transistor level schematics we may use Metal2 on the symbol level schematics. This is shown below and the top of the next page (where the inverter is used in a ring oscillator). Note that you can define node, connector, part, and device text for the schematic level on differing levels so that you won’t see the transistor level labeling text if you view these layers. Again there are all kinds of possibilities when making schematics.




LASI 6.0 Cell: RINGOSC Rank : 3 Directory : C:\Lasi6\W2uchip
Help Read Print Sys Save Cell List Undo Left Up Dn Right Fit Cntr Xpnd Zoom Last Draw
Menu 2
lDrw sDrw
Set rDrw
Outl Full
Make Smsh
Step Res
Dpth Cap
tLyr tSiz
sWin rWin
Cmd Grid
wGrd dGrd
View Open
Obj Text
Add Del
Get Put
fGet fPut
cGet cPut
tGet tPut
aPut aGet
qMov wMov
Mov Flp
Rot uDup
ReSz Snap
OvSz Orig
Text Ref. Pt.
x=2225 y=-500
Using Layer Table
wGrd=25um dGrd=25um Obj=TEXT Layr=NTXT Size=2.25um
5 Cells 0 Boxes 5 Paths 12 Vtx